

FLEX CIRCUIT SUBSTRATE FOR AN INTEGRATED CIRCUIT PACKAGE

This application claims priority under 35 U.S.C. §119 based upon Provisional Patent Application No. 60/125,735, filed Mar. 23, 1999.

FIELD OF THE INVENTION

The present invention relates generally to integrated circuit packages and more particularly to a method of fabricating flex circuit substrates.

BRIEF DESCRIPTION OF RELATED ART

As the demand for cheaper, faster and lower power consuming integrated circuits increases, so must the device packing density at the circuit board level. Not only have techniques continually evolved to meet the demand for minimizing dimensions of the transistors and of the electrical interconnections which integrate semiconductor devices, but also the packaging technology has advanced, resulting in smaller integrated circuit packages with improved electrical and thermal performance.

Ball Grid Array (BGA) and many Chip Scale Packages (CSP) are integrated circuit packages which are assembled to an external circuit board using an array of solder balls confined within the area of the package. The solder balls are electrically connected to an external circuit board, and to the chip through vias and conductor traces in the package substrate. An example of an area array package is shown in FIG. 1a and is compared to a leaded package as illustrated in FIG. 1b. With area array packages, such as the CSP depicted in FIG. 1a, solder balls 101 eliminate the protruding leads 121 in FIG. 1b of leaded packages, and a printed circuit substrate 102 supports the die and provides electrical interconnection between the die and solder balls. The circuit board replaces the die support pad 122 and the internal lead frame 123 of leaded packages in FIG. 1b, thereby providing a more compact package. In addition, improved performance is realized by lower inductance of the shorter interconnection between the chip and the external circuit board.

Integrated circuit chips 104 are electrically connected to the interconnect circuitry on the substrate either by wire bonding or by flip chip 103 connections. Substrates typically are of rigid printed wiring board construction, or for smaller and more closely spaced circuits, the interconnections are made of an unsupported flexible (flex) circuit construction. Electrical connection between the printed circuitry 105 on the chip side of the substrate to the external contact solder balls on the opposite side is typically achieved by conductive vias 106 through the substrate.

Conventional fabrication of printed circuits is achieved by preparing an enlarged-scale artwork master of a circuit pattern and conductor paths, and then the enlarged-scale artwork master is photographically reduced to the desired size. Screens and masks are fabricated according to the reduced circuit pattern for application with photoresist materials. Processes including etching, screening, plating, laminating, vacuum deposition, via hole formation, and protective coating application are used to fabricate both supported printed circuits and unsupported flexible circuits.

Substrates for area array packages on flex circuits are most commonly fabricated on a dielectric polymer base film in reel or sheet format by applying a copper metal to both surfaces. The metal conductors may be a thin foil bonded to the base film, or may be vapor deposited and subsequently plating to the necessary thickness. Interconnect traces and

contact pads are patterned and etched in the metal. Several techniques are known for electrically interconnecting the conductors and the contacts on either side of the substrate. Vias are typically formed by mechanical punching or by laser ablation, and the vias are filled with a conductor by plating, by metal deposition during the film metallization, or by filling with conductive pastes. Completing fabrication of the circuits includes plating a layer of nickel and a thin film of gold over the conductors to provide environmental protection and to support solder contacts. The final step is application of a solder mask coating to control the solder run out.

All of these fabrication techniques require multiple plating and etching steps, or in the case of laser ablation where one via is formed at a time, the repetitive process is time consuming. The via forming steps require extensive cleaning and adhesion treatment prior to metallization. Further, the existing techniques for making conductive vias suffer from difficulties in making the through holes consistently conductive, and in aligning the top and bottom circuits to the vias. Via conductivity failures occur either as opens or as intermittent failures from thin conductor walls which open during thermal excursions due to expansion mismatch between the conductor and substrate, from incompletely coating by vapor deposition, from air pockets entrapped as metal is plated from both sides, from fatigue failures of the thin conductors, from marginal conductivity of the filling material, and from marginal contact due to misalignment.

It is accordingly desirable to provide a flex circuit and a method of fabrication that permits high volume production of reliable flex circuit substrates for integrated circuit area array packages in which the technique eliminates the reliability issues identified with current processes, which minimizes the specific tooling required for each circuit design, and which does not have the need for costly vapor deposition or multiple laser drilling steps.

SUMMARY OF THE INVENTION

The principal object of the present invention is to provide an intermediate structure for flex circuits including reliable conductive vias attached to conductors on both surfaces of a dielectric film. It is further an object of this invention to provide a method for fabricating a flex circuit substrate for integrated circuit area array packages having reliable, metal conductor vias which are easily aligned to the circuitry on both surfaces of the substrate, and a method which is amenable to mass production.

In accordance with one aspect of the current invention, a plurality of conductive vias are formed in a base dielectric film having a copper film adhered to the major surfaces of the dielectric film. Sites corresponding to conductive vias in a flex circuit are patterned on the first surface, and the copper film etched to expose the via site. The photoresist is removed and the copper serves as a mask for etching the dielectric film, preferably a polyimide based polymer. The exposed polymer is etched to create a plurality of cylindrical apertures which terminate at the copper film on the second surface of the dielectric. The polymer is etched vertically and to a lesser extent is etched horizontally leaving an overhanging cusp of copper on the first surface. A fluid force is used to stretch-form the copper on the second surface into the apertures so that it terminates on the plane of the copper film on the first surface. Using the formed, intact copper layer on the second surface as the cathode, copper is electroplated from the cathode to fill any space between the copper lined via and the copper film on the first surface. The